Amendments to the Specification:

Please amend the specification as follows:

Please replace paragraph 0015 with the following rewritten paragraph:

An object of the present invention is to provide a strained active semiconductor layer MISFET in which the ~~abovementioned U-shaped dislocation~~ U-shaped dislocation described later is eliminated, the abnormal off-leakage current that occurs with a short gate is suppressed, and the power consumption is low even with a short gate.

Please replace paragraph 0032 with the following rewritten paragraph:

Supposing that only a U-shaped dislocation of length a were distributed at an area density b, then the probability of this U-shaped dislocation not spanning the source/drain of a MISFET having gate length L_G and gate width W_G would be 1 when $L_G > a$, and ~~$\exp\{-b W_G (a-L_G)\}$~~ $\exp\{-b W_G (a-L_G)\}$ when $L_G < a$.

Please replace paragraph 0033 with the following rewritten paragraph:

When it is considered that U-shaped dislocations having various lengths ai are actually distributed at area densities bi, then the probability that no U-shaped dislocations will span the source/drain of a MISFET can be written as follows: ~~$\Pi(L_G<ai)\exp\{-b_i W_G (ai-L_G)\}$~~ $\Pi(L_G<ai)\exp\{-b_i W_G (ai-L_G)\}$. In this expression, $\Pi(L_G<ai)$ signifies calculating the product of the sequence ~~$\exp\{-b_i W_G (ai-L_G)\}$~~ $\exp\{-b_i W_G (a_i-L_G)\}$ for all $L_G<ai$.

Please replace paragraph 0034 with the following rewritten paragraph:

Therefore, more than one U-shaped dislocation spans the source/drain of the MISFET, and the probability of an abnormal off-leakage current occurring becomes ~~$1-\Pi(L_G<ai)\exp\{-b_i W_G (ai-L_G)\}$~~ $1-\Pi(L_G<a_i)\exp\{-b_i W_G (a_i-L_G)\}$.

Please replace paragraph 0043 with the following rewritten paragraph:

FIGS. 34A and 34B show the concentration distribution of the impurity after heat treatment. The depth of maximum impurity concentration immediately after ion implantation

is the same as the depth of maximum impurity concentration after heat treatment. The reason for this is that the diffusion rate of the impurity decreases and approaches the original concentration distribution as the concentration of the impurity increases. Specifically, $T_p = R_p$, where T_p is the depth of maximum impurity concentration in the source/drain of finished MISFET. Consequently, when the film thickness of the strained layer is set to $2T_p$ or less as in the present invention ~~(wherein T_p is the depth of maximum impurity concentration in the source/drain)~~, a dislocation due to ion implantation is not formed in the strained layer. There is therefore no growth of U-shaped dislocations around these nuclei in the strained layer, and hence no abnormal off-leakage currents in a MISFET that has a short gate.

Please replace paragraph 0056 with the following rewritten paragraph:

FIGS. 3A through 3C, FIGS. 4A through 4C, and FIGS. 5A and 5B are sectional views showing the sequence of steps in the method for manufacturing a ~~MSIFET~~ MISFET according to a second embodiment of the present invention. First, a strained Si layer 2 is epitaxially grown on the base SiGe layer 1. The film thickness of this strained Si layer 2 is set to $2T_p$ or less, where T_p is the depth at which the impurity concentration of the source/drain of the final MISFET is at maximum (FIG. 3A). A gate insulating film 3 and a gate electrode film 4 are then grown thereon (FIG. 3B), after which patterning is performed, and a gate insulating film 3a and a gate electrode 4a having a length of 0.4 μm or less are formed (FIG. 3C).